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Question Paper Code : 80098

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019

Fourth Semester

Computer Science and Engineering

CS 8491 – COMPUTER ARCHITECTURE

(Common to Information Technology/Computer and Communication Engineering)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Amdahl's law.

2. Suppose that we are considering an enhancement to the processor of a server system used for Web Serving. The new CPU is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement?

3. Convert $(1.00101)_2$ to decimal.

4. Perform subtraction by two's complement method : 100 – 110000.

5. Convert the following code segment in C to MIPS instructions, assuming all variables are in memory and are addressable as offsets from $t0:

   $a = b + e;$ $c = b + f;$

6. Write down the five stages of instruction executions.

7. List the four multicore systems.

8. What is shared memory multiprocessor?

9. Draw the basic structure of a memory hierarchy.

10. How many total bits are required for a direct-mapped cache with 16KB of data and 4-word blocks, assuming a 32-bit address?

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PART B — (5 × 13 = 65 marks)

11. (a) (i) Describe the different types of addressing mode with example. (7)

(ii) Explain the components of a computer with the block diagram in detail. (6)

Or

(b) (i) Explain the eight ideas of the Computer architecture which empowered the computer design over the past decades. (7)

(ii) Tabulate the difference between the RISC and CISC processor. (6)

12. (a) Calculate the following problems using BOOTH'S ALGORITHM (13)

(i) (+13) × (–6)

(ii) (+13) × (+6)

(iii) (–13) × (–6)

(iv) (-13) × (+6)

Or

(b) Calculate 10011 (–13) × 01011 (+11) using Signed-Operand Multiplication. (13)

13. (a) Explain the basic MIPs implementation with necessary multiplexers and control lines. (13)

Or

(b) Explain how the instruction pipeline works? What are the various situation where an instruction pipeline stalls? Illustrate with an example. (13)

14. (a) Explain in detail Flynn's classification of parallel hardware. (13)

Or

(b) Discuss the principle of hardware multithreading and elaborate its types. (13)

15. (a) Explain the various mapping functions that can be applied on cache memories in detail. (13)

Or

(b) (i) With a neat sketch explain the working principle of DMA. (8)

(ii) Explain about input-output processor (IOP) (5)

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PART C — (1 × 15 = 15 marks)

16. (a) In a small town, there are three temples in a row and a well in front of each temple. A pilgrim came to the town with certain number of flowers.

Before entering the first temple, he washed all the flowers he had with the water of well. To his surprise, flowers doubled. He offered few flowers to the God in the first temple and moved to the second temple. Here also, before entering the temple he washed the remaining flowers with the water of well. And again his flowers doubled. He offered few flowers to the God in second temple and moved to the third temple. Here also, his flowers doubled after washing them with water. He offered few flowers to the God in third temple.

There were no flowers left when pilgrim came out of third temple and he offered same number of flowers to the God in all three temples. What is the minimum number of flowers the pilgrim had initially (X)? And find the value of (X/3) using Restoring Division method? How many flower did he offer to each God (Y)? And find the value of (Y/3) using Non-Restoring Division method? (15)

Or

(b) (i) You have been asked to design a cache with the following properties : (8)

(1) Data words are 32 bits each

(2) A cache block will contain 2048 bits of data

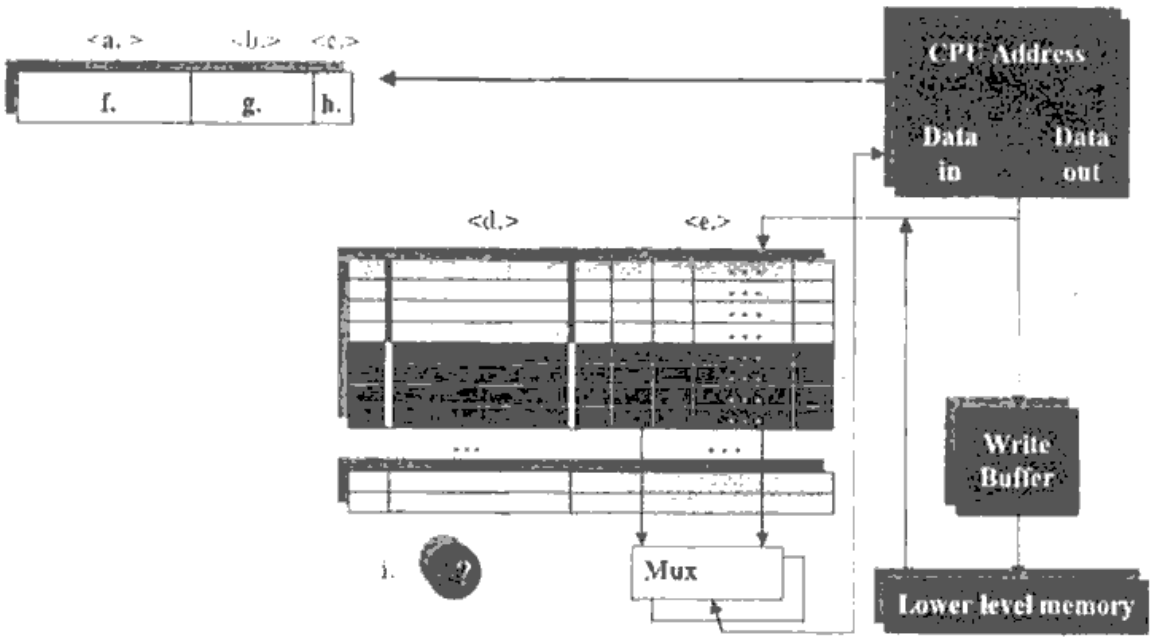
(3) The cache is direct mapped

(4) The address supplied from the CPU is 32 bits long

(5) There are 2048 blocks in the cache

(6) Addresses are to the word.

(ii) In the below picture, there are 8 fields (labeled a, b, c, d, e, f, g, and h), you will need to indicate the proper name or number of bits for a particular portion of this cache configuration. Explain the process of accessing data using this design. (7)



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